Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A method for controlling the common-mode output voltage in a fully differential amplifier, the method comprising:
comparing a sensed common-mode output voltage of the fully differential amplifier to a reference voltage;
generating an error signal representing the difference between said sensed common-mode output voltage and said reference voltage; and
utilizing said error signal to control the body voltage of one or more FET devices included within the fully differential amplifier until said sensed common-mode output voltage is in agreement with said reference voltage.

[c2] 2.The method of claim 1, further comprising clamping said one or more FET devices so as to prevent activation of body-to-diffusion diodes therein.

[c3] 3.The method of claim 2, further comprising configuring a frequency compensating device in communication with said one or more FET devices so as to set a dominant pole in a feedback loop defined by said error signal and said one or more FET devices.

[c4] 4.The method of claim 1, wherein said one or more FET devices further comprise a pair of PFET load devices coupled to a respective pair of output terminals of the fully differential amplifier.

[c5] 5.The method of claim 1, wherein said one or more FET devices further comprise a PFET device included in a reference current mirror of the fully differential amplifier.

[c6] 6.The method of claim 1, wherein said one or more FET devices further comprise an NFET device included in a bias current mirror of the fully differential amplifier.

[c7] 7.An apparatus for controlling the common-mode output voltage in a fully differential amplifier, comprising:
a sensing scheme for determining a sensed common-mode output voltage of the fully differential amplifier;
an error amplifier for comparing said sensed common-mode output voltage to a reference voltage, said error amplifier configured to generate an error signal representing the difference between said sensed common-mode output voltage and said reference voltage; and
said error signal coupled to a body terminal of one or more FET devices included within the fully differential amplifier so as to control the body voltage thereof until said sensed common-mode output voltage is in agreement with said reference voltage.

[c8] 8.The apparatus of claim 7, further comprising a clamping device coupled to said one or more FET devices so as to prevent activation of body-to-diffusion diodes therein.

[c9] 9.The apparatus of claim 8, further comprising a frequency compensating device coupled to said one or more FET devices so as to set a dominant pole in a feedback loop defined by said error signal and said one or more FET devices.

[c10] 10.The apparatus of claim 7, wherein said one or more FET devices further comprise a pair of PFET load devices coupled to a respective pair of output terminals of the fully differential amplifier.

[c11] 11.The apparatus of claim 7, wherein said one or more FET devices further comprise a PFET device included in a reference current mirror of the fully differential amplifier.

[c12] 12.The apparatus of claim 7, wherein said one or more FET devices further comprise an NFET device included in a bias current mirror of the fully differential amplifier.

[c13] 13.The apparatus of claim 8, wherein said clamping device comprises a diode.

[c14] 14.The apparatus of claim 8, wherein said frequency

compensating device comprises a capacitor.

[c15] 15.A method for controlling the common-mode output voltage in a fully differential amplifier, the method comprising:
comparing a sensed common-mode output voltage of the fully differential amplifier to a desired common-mode output voltage;
generating an error signal representing the difference between said sensed common-mode output voltage and said reference voltage;
utilizing said error signal as an input to a coarse feedback loop, said coarse feedback loop coupled to a reference current mirror in the fully differential amplifier; and
utilizing said error signal as an input to a fine feedback loop, said fine feedback loop configured to control the body voltage of one or more FET devices included within said reference current mirror until said sensed common-mode output voltage is in agreement with said desired common-mode output voltage.

[c16] 16.The method of claim 15, wherein said coarse feedback further comprises a digital up/down counter having said error signal as an input thereto, said up/down counter generating an n-bit binary word inputted to a digital-to-analog (DAC) converter, said DAC in turn generating an output coupled to said reference current mir-

ror in the fully differential amplifier.

[c17] 17.The method of claim 16, further comprising:
generating a body reference voltage;
said body reference voltage coupled to body terminals of a pair of PFET load devices in turn coupled to a respective pair of output terminals of the fully differential amplifier; and
said body reference voltage further coupled to a body terminal of a PFET device included in said reference current mirror when the fully differential amplifier is in a coarse feedback mode of operation.

[c18] 18.The method of claim 17, wherein said body reference voltage is decoupled from said body terminal of said PFET device included in said reference current mirror when the fully differential amplifier is in a fine feedback mode of operation.

[c19] 19.The method of claim 17, wherein said body reference voltage is generated through a resistive divider and an operational amplifier configured as a voltage follower.

[c20] 20.The method of claim 15, further comprising clamping said reference current mirror so as to prevent activation of body-to-diffusion diodes therein.

[c21] 21.The method of claim 20, further comprising configur-

ing a frequency compensating device in communication with said reference current mirror so as to set a dominant pole in said fine feedback loop.

[c22] 22.An apparatus for controlling the common-mode output voltage in a fully differential amplifier, comprising:
a sensing scheme for determining a sensed common-mode output voltage of the fully differential amplifier;
an error amplifier for comparing said sensed common-mode output voltage to a reference voltage, said error amplifier configured to generate an error signal representing the difference between said sensed common-mode output voltage and said reference voltage;
said error signal utilized as an input to a coarse feedback loop, said coarse feedback loop coupled to a reference current mirror in the fully differential amplifier; and
said error signal further utilized as an input to a fine feedback loop, said fine feedback loop configured to control the body voltage of one or more FET devices included within said reference current mirror until said sensed common-mode output voltage is in agreement with said desired common-mode output voltage.

[c23] 23.The apparatus of claim 22, wherein said coarse feedback further comprises a digital up/down counter having said error signal as an input thereto, said up/down counter generating an n-bit binary word inputted to a

digital-to-analog (DAC) converter, said DAC in turn generating an output coupled to said reference current mirror in the fully differential amplifier.

[c24] 24.The apparatus of claim 23, further comprising:
a body reference voltage generator;
an output of said body reference voltage generator coupled to body terminals of a pair of PFET load devices in turn coupled to a respective pair of output terminals of the fully differential amplifier; and
said output of said body reference voltage generator further coupled to a body terminal of a PFET device included in said reference current mirror when the fully differential amplifier is in a coarse feedback mode of operation.

[c25] 25.The apparatus of claim 24, wherein said body reference voltage is decoupled from said body terminal of said PFET device included in said reference current mirror when the fully differential amplifier is in a fine feedback mode of operation.

[c26] 26.The apparatus of claim 24, wherein said body reference voltage is generated through a resistive divider and an operational amplifier configured as a voltage follower.

[c27] 27.The apparatus of claim 22, further comprising a

clamping device to said reference current mirror so as to prevent activation of body-to-diffusion diodes therein.

[c28] 28.The apparatus of claim 27, further comprising a frequency compensating device in communication with said reference current mirror so as to set a dominant pole in said fine feedback loop.